Modeling ABB's HVDC/CCC into the CEPEL Simulation Package

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Summary

This paper describes the results of the implementation of an HVDC/CCC model into the CEPEL simulation package. Results on power flow, transient stability, small signal analysis and control design are shown. The implementation and validation of results were made by CEPEL with the help of ABB Power Systems. Comparisons are made on the performances of CCC, conventional converters and pseudo CCC models. The CCC steady-state and dynamic performances proved to be superior to those of conventional converters when the connected AC systems are weak.

Keywords: Capacitor Commutated Converter - CCC - Long distance transmission - HVDC - Power Flow - Transient stability - Controller design.

1. Introduction

This paper describes the results of a joint development work, carried out by CEPEL and ABB Power Systems, under contract by ABB Power Systems, to model the recently proposed HVDC/CCC (Capacitor Commutated Converters) into the simulation software package of CEPEL. This simulation package comprises programs for power flow (ANAREDE)[1], transient stability (ANATEM)[2,3] and small signal stability analysis (PacDyn)[4,5], and employ methods which reflect the state of art in the field. The implementation was carried out in CEPEL while the tests and validation were made by both parties.

An HVDC/CCC is a conventional converter provided with Commutation Capacitor in series with the valves[6,7]. The HVDC/CCC can be combined with a small actively tuned AC filter to create a favorable transmission system. This concept results in large savings in reactive power compensation devices needed at the converter stations. The reactive power consumption of a conventional converter station can be as high as 60% of the active power being transmitted, while in the new design this consumption is brought down to 15% or less.

Full prototype testing of this new concept has been carried out by ABB, who is now ready to supply it to utilities' new installations. Several projects involving large power imports from neighbor countries to Brazil are currently being studied for urgent commissioning. The HVDC/CCC concept is being considered by ABB as a viable technical and economic transmission alternative to these projects. In order to promote early studies of this new concept, ABB Power Systems has contracted CEPEL to include the CCC converter models into the CEPEL simulation package, in use by most of the Brazilian utilities.

The results presented in this paper include comparisons with PSS/E software, from Power Technologies Inc., provided by ABB.

2. Development Phases of the Work

The work started with the preparation of a detailed report by CEPEL on the modeling of conventional HVDC links in the CEPEL software. This report was sent to ABB together with the user manuals of the programs involved, and served as the initial contact of ABB with the CEPEL software.

The following step was the technical visit to CEPEL, for three weeks, of a senior ABB specialist on HVDC technology. Under a confidentiality agreement, CEPEL received several reports describing the HVDC/CCC equations and control circuitry. By the end of this visit, the CEPEL team was already sufficiently familiar with the CCC

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modeling for steady state and transient stability analysis. Also, considerable progress had been made on the implementation of the CCC model into the ANAREDE program. The work on the other two programs had already been started.

Communication between CEPEL and ABB have, from then onwards, been made by FAX and e-mail. Valuable support was also given by an ABB engineer stationed in Rio de Janeiro.

During all stages of this work there was a large effort in validating the HVDC/CCC models in the CEPEL software. A description of the different ways in which this validation was carried out is given below:

- The power flow results obtained by ANAREDE, regarding the complex HVDC/CCC relationships, were verified through Matlab simulations of the CCC equations.

- The ANATEM final steady-state values, obtained following a permanent line outage, matched the ANAREDE results produced by the removal of the same transmission line.

- The dynamic responses obtained by the ANATEM and PacDyn programs showed a perfect matching, following the application of a small disturbance (0.1 %) in the current order of the master control.

- The results produced by ANATEM for large disturbances were seen to also match very well those obtained by PSS/E (Power Technologies Inc. software) and provided by ABB Power Systems. These comparisons involved the application of three disturbances: a 10% step in the current order, an AC fault at the rectifier side and another AC fault at the inverter side.

After the validation work was completed, engineering studies were carried out in CEPEL, under contract by ABB, to assess the cost-effectiveness of a few transmission projects in South-America.

3. Test Systems

Several test systems were studied during the implementation work and validations tests. This paper will present the results of two small test systems. The first test system was modeling a cable transmission system with strong AC networks to verify the control functions. The second test system was modeling a realistic Back-to-Back transmission with a very weak inverter AC system. The basic data of the two test systems are shown in Appendix 1.

The steady-state equations for the HVDC/CCC converter are more complex than those for the conventional HVDC converter, due to the presence of the commutation capacitor. The expressions for the converter variables are not explicit any longer, and require an iterative process to be obtained.

The basic data for the conventional and CCC converter examples of this paper are the same, except for the commutation capacitor. If the commutation capacitor is set to infinity, the CCC model becomes equivalent to the conventional converter model.

The CCC controls were provided by ABB Power Systems and are more complex than the conventional HVDC controls. They were modeled in detail in ANATEM and PacDyn using the user defined controller modeling capability of these programs.

4. Power Flow Results

This section describes ten power flow results of the ANAREDE program for the two test systems described in the Appendix 1. Each test system has five power flow cases, each one corresponding to a different control mode of operation:

1- **Normal** - The firing angle (α) at rectifier, commutation margin angle (γ) at inverter, rectifier DC voltage (U_d) and DC current (I_d) are specified.

2- **Fixed tap at rectifier** - The tap (Tap_r) at rectifier, commutation margin angle (γ) at inverter, rectifier DC voltage (U_d) and DC current (I_d) are specified.

3- **Fixed tap at inverter** - The firing angle (α) at rectifier, commutation margin angle (γ) at inverter, tap (Tap_i) at inverter and DC current (I_d) are specified.

4- **Fixed tap at rectifier and inverter** - The tap (Tap_r) at rectifier, commutation margin angle (γ) at inverter, tap (Tap_i) at inverter and DC current (I_d) are specified.

5- **Reduced AC voltage operation** - The tap (Tap_r) at rectifier, firing angle at rectifier (α), tap (Tap_i) at inverter and a lower value for DC current (equal to current order minus current margin of 0.02 pu) are specified.

The Table 1 below summarizes this description:

TABLE 1

Case	Tap_r	Tap_i	α	γ	U_d	I_d
1 - Normal	C	C	S	S	S	S
2- Fixed tap at rectifier	S	C	C	S	S	S
3- Fixed tap at inverter	C	S	S	S	C	S
4- Fixed tap at rectifier and inverter	S	S	C	S	C	S
5- Reduced voltage operation	S	S	S	C	C	S

where:
C - indicates a calculated variable
S - indicates an user specified variable

The power flow results for Test System 1 and Test System 2 are shown in Appendix 2.

Another important power flow control mode of operation, still to be implemented, is the CCC inverter firing control to

keep constant the AC bus voltage, irrespective of system loading. This CCC control mode is equivalent to having a SVC at the inverter terminals, and may enhance operation in some cases.

5. Small Signal Stability and Control Design Results

PacDyn allows small signal stability assessment for systems containing CCC converters. Only a brief overview of the validation results are given in this section, due to the ample scope and limited space available in this paper.

The Figures 1, 2 and 3 pictures the comparative results of rectifier firing angle, inverter firing angle and rectifier DC current for the transient stability (ANATEM) and the small signal stability (PacDyn) programs, following a step of 1% in the current order of master control of the Test System 1. The step is applied at 100 ms and removed at 400 ms.

The difference between the results of the two programs are just visible, due to the effect of non-linearities for the 1% step disturbance. For smaller disturbances, the simulation of the two programs coincide perfectly.

The full eigensolution for the Test System 1 is shown below:

Eigenvalues

```
          -1065.9
          -1008.8
          -1000.0
          -503.12
          -378.02
-25.046  ± j 314.30  (ξ=7.94%)
-57.902  ± j 104.67  (ξ=48.4%)
          -24.741
          -9.9181
```

where ξ indicates the damping factor of the oscillatory eigenvalues. Note that there is a 50 Hz (314.3 rad/s) oscillation mode with a damping of 7.94 %, which is visible in the plots shown in Figures 1 and 3.

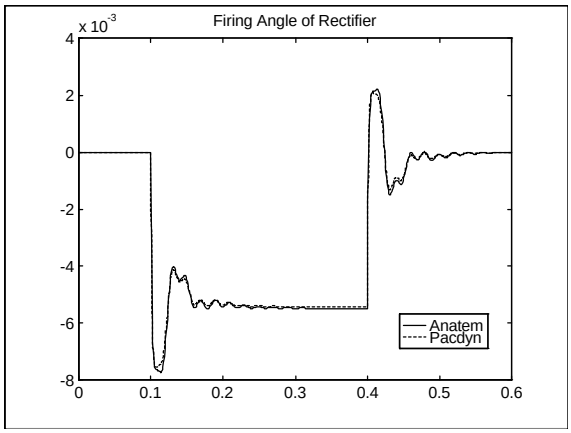

Figure 1 - Rectifier Firing Angle (α_1).
Small Disturbance Results for Test System 1

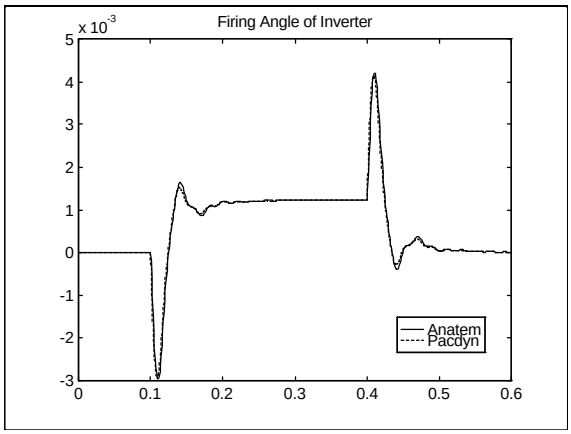

Figure 2 - Inverter Firing Angle (α_2).
Small Disturbance Results for Test System 1.

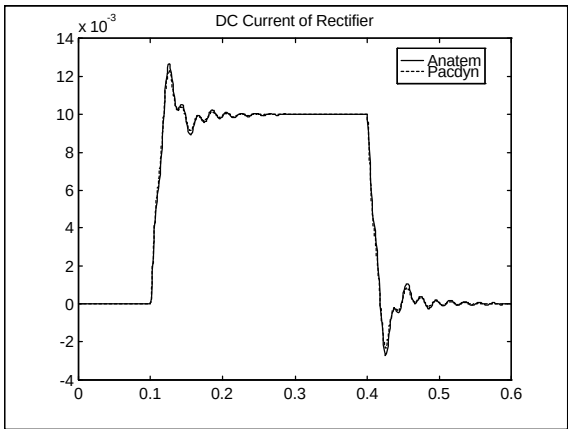

Figure 3 - Rectifier DC Current (I_{dc1}).
Small Disturbance Results for Test System 1.

Figures 4 to 6 show Root Locus results for changes in the gains of the PI controller for the rectifier current control.

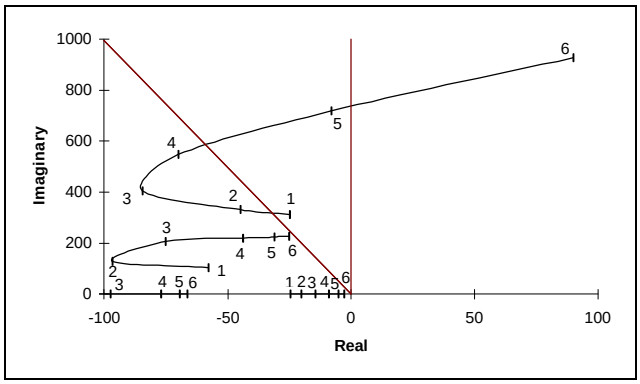

Figure 4 - Root Locus for changes in the Proportional Gain (Kp) of the Rectifier Current Control, for Test System 1.

Symbols in the plot and associated gains:

1 - Kp = 35 (Base Case)	2 - Kp = 70
3 - Kp = 140	4 - Kp = 280
5 - Kp = 560	6 - Kp = 1120

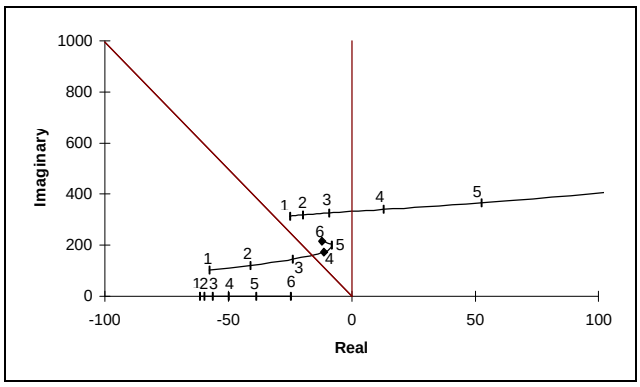

Figure 5 - Root Locus for changes in the Integral Gain (Ki) of the Rectifier Current Control, for Test System 1.

Symbols in the plot and associated gains:

1 - Ki = 3333.33 (Base Case)	2 - Ki = 6666.66
3 - Ki = 13333.3	4 - Ki = 26666.6
5 - Ki = 53333.3	6 - Ki = 106666.

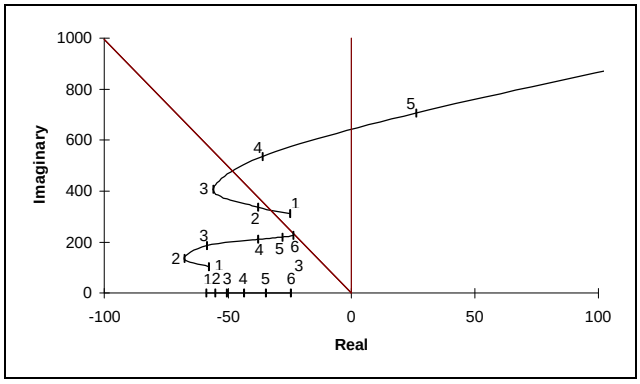

Figure 6 - Root Locus for a simultaneous change in the Proportional Gain (Kp) and Integral Gain (Ki) of the Rectifier Current Control, for Test System 1.

Symbols in the plot and associated gains:

1 - Kp = 35	Ki = 3333.33 (Base Case)
2 - Kp = 70	Ki = 6666.66
3 - Kp = 140	Ki = 13333.3
4 - Kp = 280	Ki = 26666.6
5 - Kp = 560	Ki = 53333.3
6 - Kp = 1120	Ki = 106666.

From these Root Locus plots it is seen that the best combination of gains is Kp = 140 and Ki = 3333.33, regarding the damping of the critical system eigenvalues.

Figures 7 and 8 show the DC current at the rectifier for two values of Kp: 140 and 560, with Ki fixed at 3333.33. Note that Figure 7, when compared to Figure 3, shows a larger initial oscillation followed by a better damped tail end. Figure 8 shows a poorly damped oscillation at about 100 Hz, as indicated by the Root Locus plot in Figure 4.

It is important to note that the optimum gain must take into account, not only the damping of the critical eigenvalues, but also the smoothness of the dynamic response for the system variables of interest. This aspect depends on the location of the transfer function zeros and poles (eigenvalues) of the system, and is more easily verified by time domain simulations.

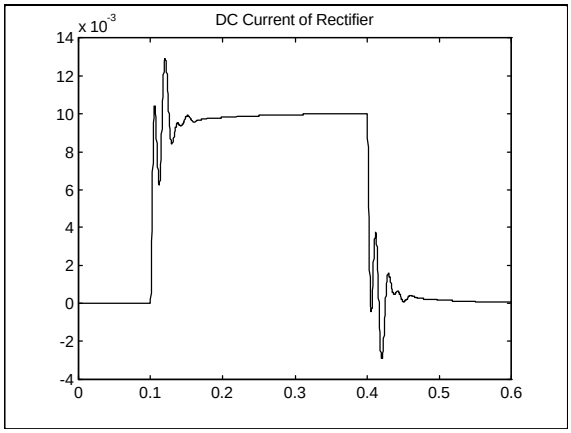

Figure 7 - Rectifier DC Current (I_{dc1}) for Kp=140 and Ki=3333.33. These control parameters correspond to point #3 of the Root Locus inFigure 4.

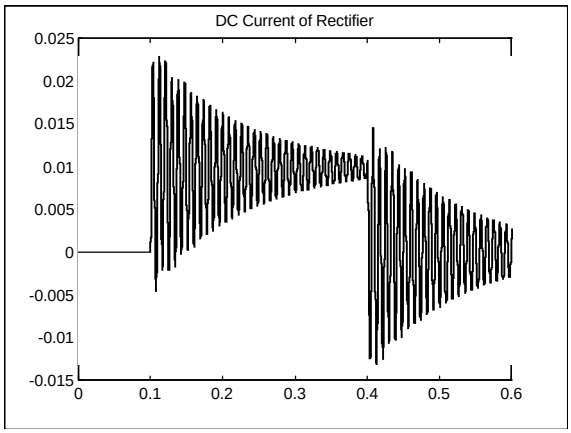

Figure 8 - Rectifier DC Current (I_{dc1}) for Kp=560 and Ki=3333.33. These control parameters correspond to point #5 of the Root Locus inFigure 4.

6. Comparison of Transient Stability Simulation Obtained by PSS/E and ANATEM Programs

The Test System 1 simulation in ANATEM was validated using the program PSS/E from Power Technologies Inc.

This validation could not be very accurately carried out, since the PSS/E results were supplied by FAX by ABB Power Systems. The results for the three chosen disturbances were, however, seen to be practically equivalent.

The Figure A3-1 in Appendix 3 is a FAX transmission copy of the PSS/E results, where the following variables are depicted: DC current order and the actual DC currents at the rectifier and inverter. The Figure A3-2 shows the ANATEM plots for the same variables and disturbance, which are seen to match well those of the PSS/E program.

7. Simulation of Severe AC Fault at Inverter Side

The results in this section relate to a three-phase fault applied to the inverter side, for both Test Systems 1 and 2. The fault was applied at 100 ms and removed at 200 ms. The

fault impedance is 0.0005 pu in 100 MVA base, which characterizes a very severe event.

The CCC behavior, for an AC fault at the inverter is now described in association with Figure 9 to Figure 13. This behavior is similar to that of a conventional HVDC converter. The requirements for reactive power during transients are smaller, however, avoiding dynamic performance problems which may occur in weak AC receiving systems.

Following the severe fault at the inverter side, the associated voltage drop causes commutation failure, which is represented in the simulation, as a zero DC voltage. This makes the DC current to rapidly rise causing the rectifier current controller to increase the firing angle in order to reduce the DC voltage and DC current.

The rectifier control action, after some time delay, causes the desired reduction in the DC current. The control induced DC current undershoot, brings the current down to zero and causes inverter blocking, which is represented in the simulation as an open circuited inverter.

The rectifier firing angle continues to reduce until the inverter deblocking. As the AC fault has not yet been removed and the AC voltage is consequently low, the inverter goes directly into a commutation failure. Due to the low DC voltage, the rectifier current order is kept at a reduced value by the VDCOL action. Following the removal of the fault at 200 ms, the DC voltage increases, the current order rises to its nominal value and the system gradually recovers. The charging of the large capacitance of DC cable impacts system recovery. A more detailed description of large cable capacitance effects can be found in [8].

All the results for Test System 1 match those obtained by PSS/E, as described in the previous section and Appendix 3.

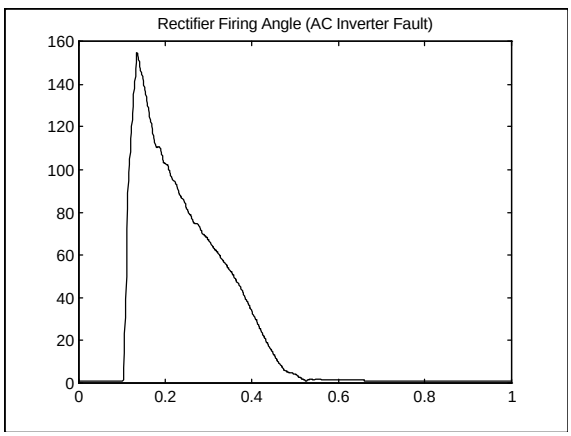

Figure 9 - Rectifier Firing Angle (α_1) for Test System 1.

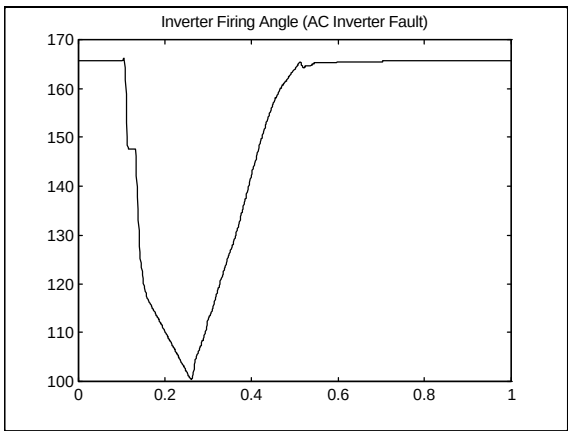

Figure 10 - Inverter Firing Angle (α_2) for Test System 1.

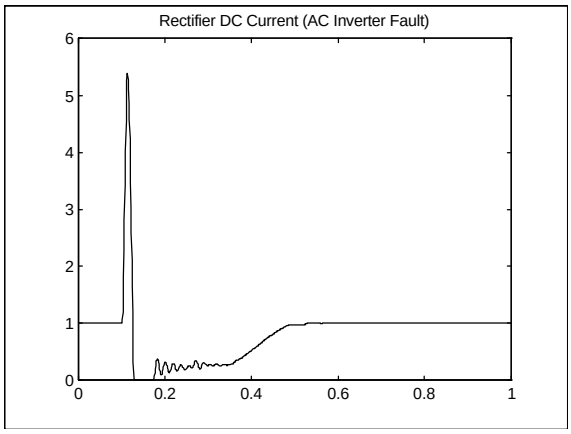

Figure 11 - Rectifier DC Current (I_{dc1}) for Test System 1.

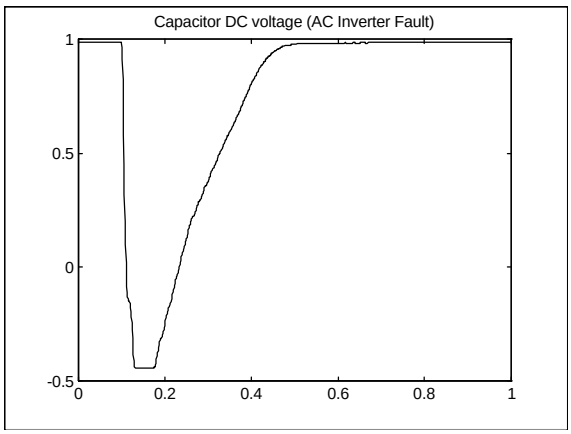

Figure 12 - Mid-line DC Voltage (V_{dc1}) for Test System 1.

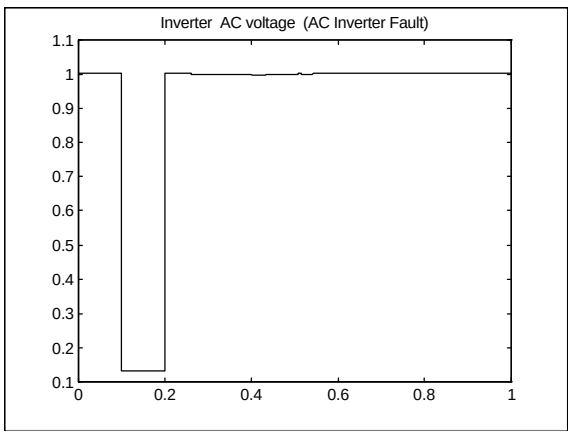

Figure 13 - Inverter AC Voltage (V_{ac2}) for Test System 1.

The current control proportional gain was increased in order to speed up the response for Test System 2. The same AC inverter fault was simulated and the corresponding plots are shown in Figure 14 to Figure 21.

As described previously for Test System 2, the inverter goes to a commutation failure after the fault which is applied at t=0.1 s, bringing the inverter voltage to zero. The DC current increases and the rectifier current control reacts to that by increasing the firing angle so as to reduce the current. In sequence, the DC current goes to zero and the converters block. The rectifier firing angle and the DC current are shown in Figure 14 and Figure 15. Figure 16 shows the rectifier and inverter DC voltages. The voltage at the rectifier becomes negative for high firing angles, in an attempt to reduce the current. As a consequence of blocking at t = 0.124 s, the DC voltage at the rectifier goes to zero. Note that the inverter voltage was already zero due to the commutation failure.

After blocking, the rectifier current control decreases the firing angle causing the rectifier and inverter deblockings at t=0.129 s and tries to keep the current to the VDCOL minimum current value adjusted to 0.345 pu (see Figure 15 and Figure 17). The DC voltage at inverter side is very low due to the practically zero inverter AC voltage (see Figure 18).

Note that the inverter deblocks because the series capacitors of the CCC inverter create an extra voltage contribution to the commutation voltages. This means that the current can continue to commutate during AC faults even at zero level of the remaining commutation voltages.

After the fault clearance at t=0.200 s, the AC and DC inverter voltages increase (the inverter firing angle is not too low - see Figure 14), causing a temporary DC current interruption from t = 0.201 s to t = 0.217 s (see Figure 20). After deblocking, the power recovers gradually (see Figure 21).

The CCC is much more competent to commutate during disturbances than the conventional converter due to the series capacitor voltage contribution to the valves. The commutation margin also increases at higher currents. This means that there is no need to impose a fast reduction of the DC current order during disturbances. However, the requirements to reduce the current and thus limit the stresses of longer duration on the valves are still valid but can be applied with a much longer time constant.

This fact can be used to improve the restart after an AC fault by maintaining the actual current order during the fault through the elimination of the fast VDCOL action. This advantage was not exploited in this study as the main purpose was to verify control functions. This fact, however, can be used to reduce the restart time in practical applications.

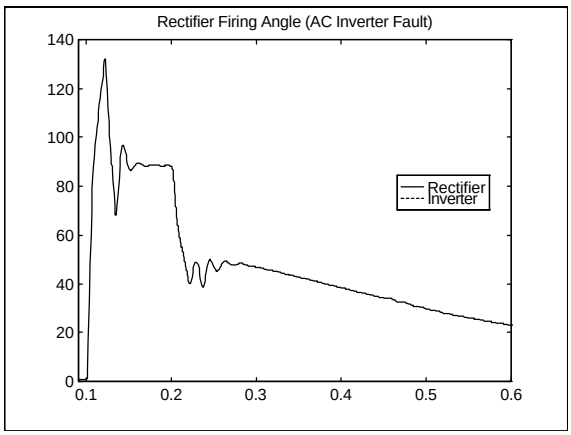

Figure 14 - Rectifier Firing Angle (α_1) for Test System 2.

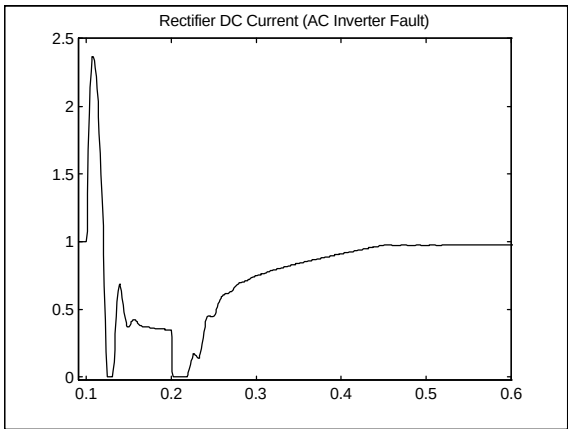

Figure 15 - Rectifier DC Current (I_{dc1}) for Test System 2.

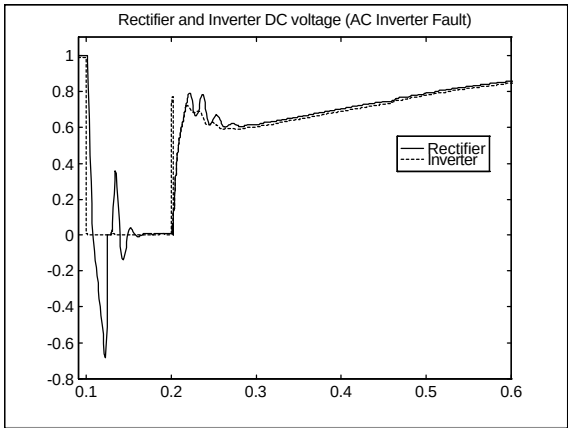

Figure 16 - Rectifier and Inverter DC Voltage (V_{dc2}) for Test System 2.

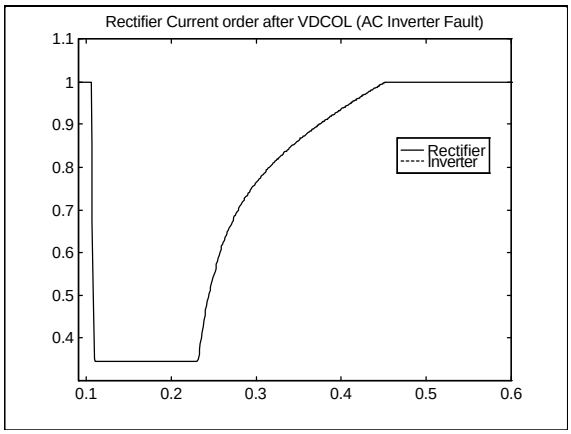

Figure 17 - Rectifier Current Order after VDCOL for Test System 2.

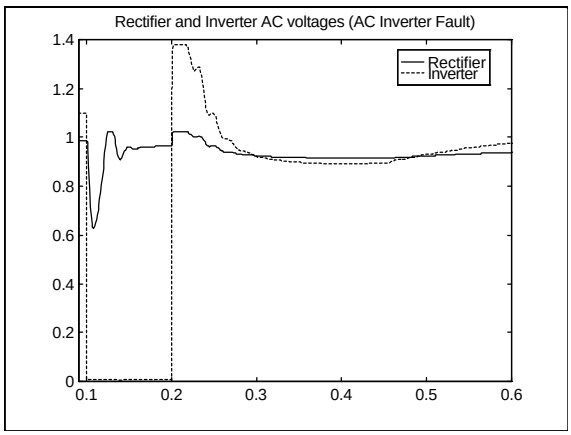

Figure 18 - Rectifier and Inverter AC Voltages for Test System 2.

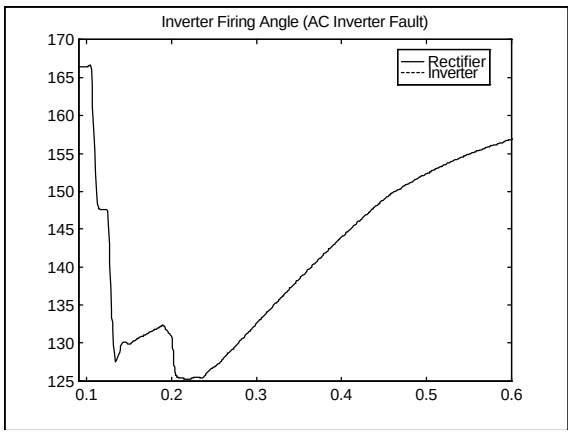

Figure 19 - Inverter Firing Angle (α_2) for Test System 2.

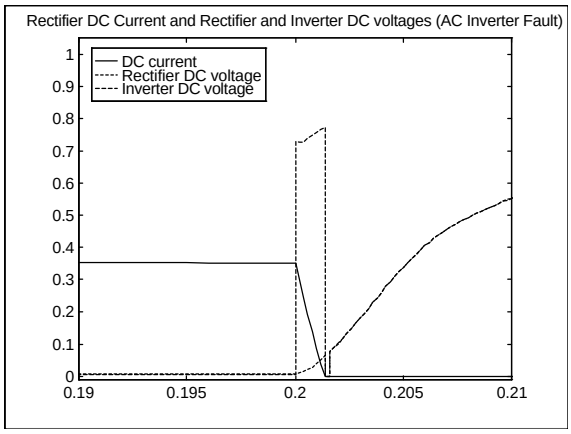

Figure 20 - Rectifier DC Current and Rectifier and Inverter DC Voltages for Test System 2.

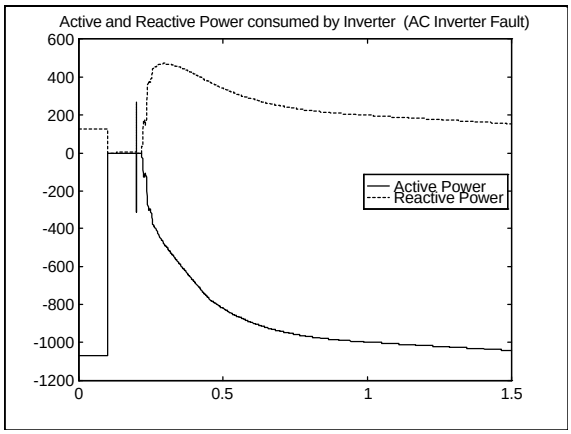

Figure 21 - Active and Reactive Power Consumed by Inverter

8. Performances of CCC, Pseudo CCC and Conventional Converter Models for Changes in Current Order

This section reports on the simulation results for Test System 1, considering three possible types of converter model: CCC, pseudo CCC and conventional HVDC converter.

The CCC model comprised the full set of detailed nonlinear equations,provided by ABB, which require iterative solution.

In the pseudo CCC model, the commutation capacitor is represented as a capacitive reactance, external to a conventional converter model. The power flow interface variables were made equivalent for both CCC and pseudo CCC by proper choice of firing angle at rectifier and extinction angle at inverter.

The conventional HVDC model had the same angles at both converters and a larger shunt capacitance to compensate for the lack of the series capacitance. The reactive demand at the converter terminals were again the same as for the other two converter models.

The same control block diagrams were used for the three converter models, considering the commutation capacitor impedance equivalent to zero when appropriate. The main control loop at the rectifier is the constant current control and at the inverter is the commutation margin control (CCC) or the minimum extinction angle control (pseudo CCC and conventional converters). Note that the commutation margin becomes equal to the extinction angle when there is no commutation capacitor.

All results in this section are for a +10% step disturbance to the DC current order applied at 0.1 s and removed at 0.4 s.

8.1 *Results for Test System 1 (CCC versus Conventional Converter)*

The step disturbance results for the CCC and conventional models are shown in Figure 22 to Figure 28. The controller parameters for both models are the same except for the PI controller at the rectifier, which had its gain reduced by one half for the conventional converter.

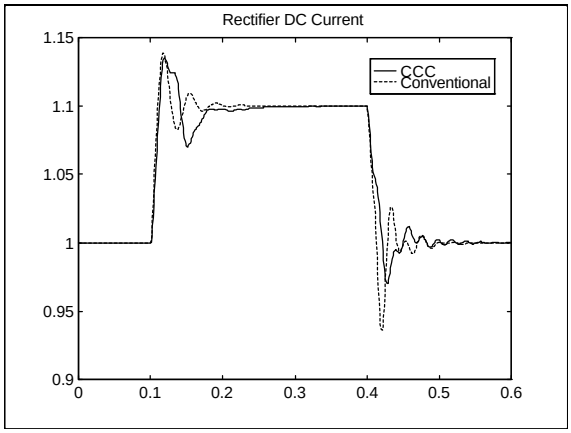

Figure 22 - Rectifier DC Current (I_{dc1}) .
Results for Test System 1: CCC versus Conventional Converter.

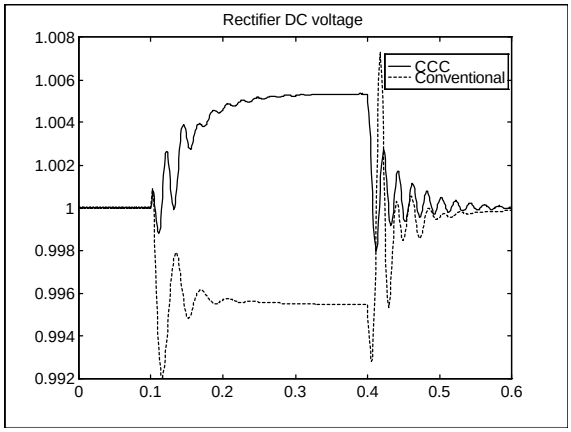

Figure 23 - Rectifier DC Voltage (V_{dc1}) .
Results for Test System 1: CCC versus Conventional Converter.

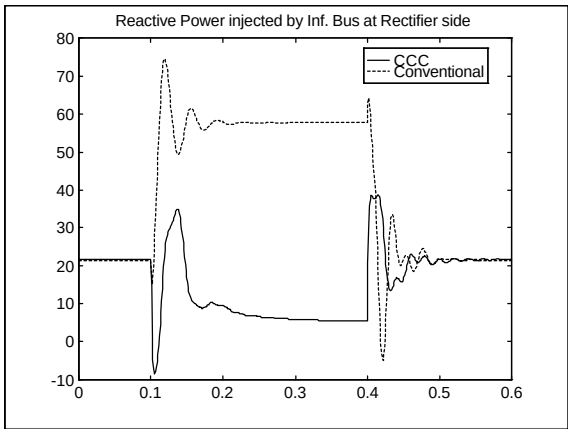

Figure 24 - Reactive Power Injected by Infinite Bus at Rectifier side (Q_{dc1}).
Results for Test System 1: CCC versus Conventional Converter.

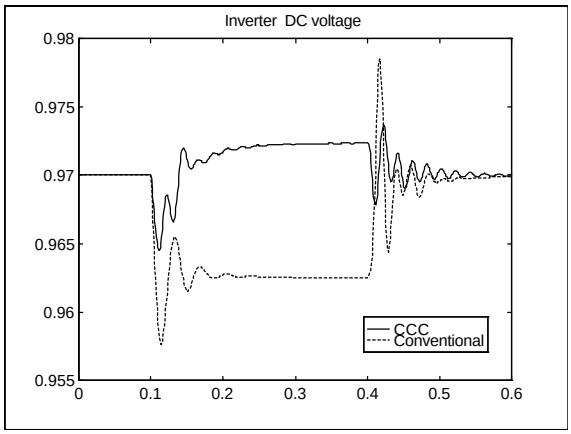

Figure 25 - Inverter DC Voltage (V_{dc2}).
Results for Test System 1: CCC versus Conventional Converter.

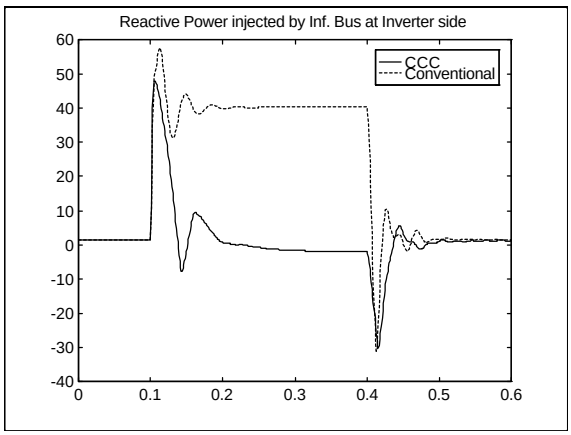

Figure 26 - Reactive Power (Q_{dc2}) Injected by Infinite Bus at the Inverter side.
Results for Test System 1: CCC versus Conventional Converter.

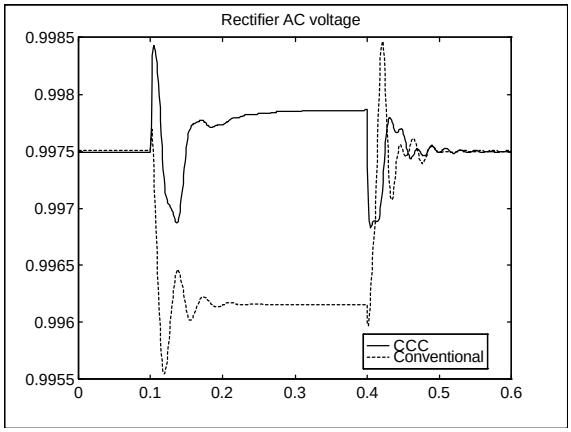

Figure 27 - Rectifier AC Voltage (V_{ac1}).
Results for Test System 1: CCC versus Conventional Converter.

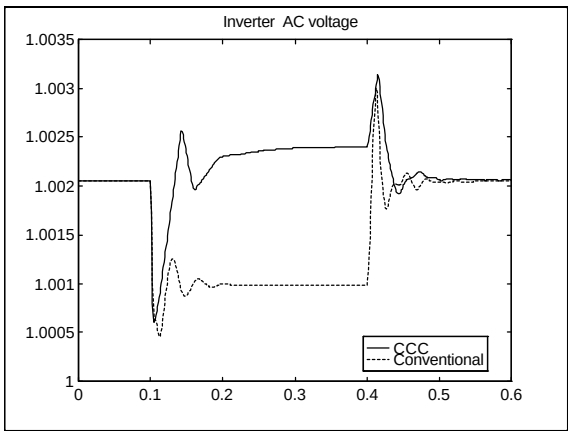

Figure 28 - Inverter AC Voltage (V_{ac2})
Results for Test System 1: CCC versus Conventional Converter.

The qualitative behavior of the CCC may be largely different from the conventional converter. This difference increases with the value of the commutation capacitor reactance. The capacitor reactance may be as large as three times the leakage reactance of the converter transformer.

When applying a positive step in the current order of the CCC, the current flowing through the commutation

capacitor increases, causing the two converters to absorb less reactive power. This causes the AC voltages at both terminals to go to higher steady-state values. The steady-state DC voltage at the inverter also rises, since the commutation margin control does not act against it.

In order to obtain the desired increase in current, the rectifier current controller lowers the firing angle in order to increase even more the DC voltage at the rectifier.

The conventional converter model shows a different steady-state characteristic, since the reactive consumption at both terminals always increases with the DC current. The AC voltages at the two terminals are therefore reduced in proportion to their SCR. The steady-state DC voltage at the inverter is also reduced, since the extinction angle control does not act against it. In order to obtain the desired increase in current, the rectifier current controller lowers or raises the firing angle in order to ensure the proper DC voltage drop between the converters.

One should note that the CCC scheme is particularly advantageous for weak receiving end systems (low SCR), since the reactive demand of the CCC reduces with the level of power transmission. This characteristic improves the system dynamic performance regarding electromechanical and voltage stability problems.

8.2 *Results for Test System 1 (CCC versus Pseudo CCC)*

The step disturbance results for the CCC and pseudo CCC models are shown in Figure 29 to Figure 35 for Test System 1. The controller parameters for both models are the same. The step responses in these figures are self-explanatory and show that, for Test System 1, the pseudo CCC has an equivalent but faster response as compared to the CCC. The behaviors of the two models are roughly equivalent due to the strong AC systems at both sides.

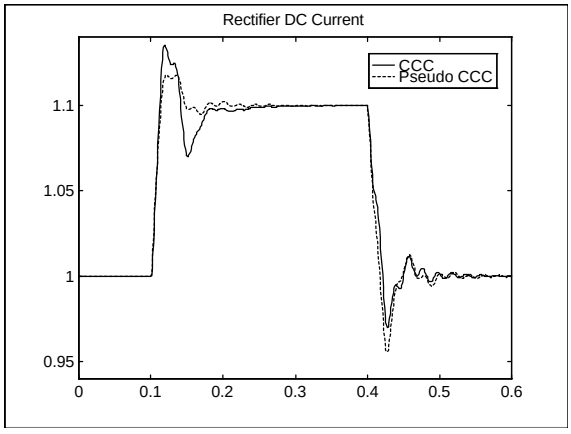

Figure 29 - Rectifier DC Current (I_{dc1})
Results for Test System 1: CCC versus Pseudo CCC.

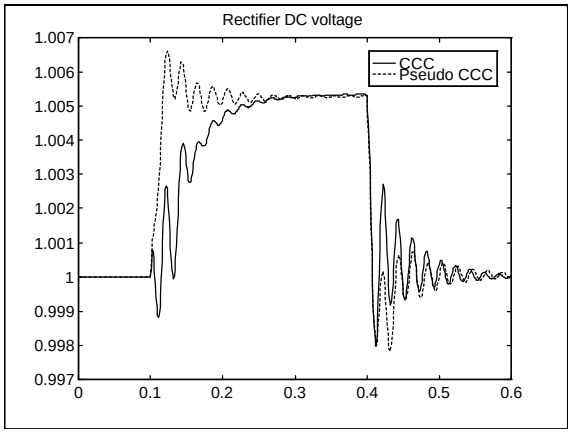

Figure 30 - Rectifier DC Voltage (V_{dc1})
Results for Test System 1: CCC versus Pseudo CCC.

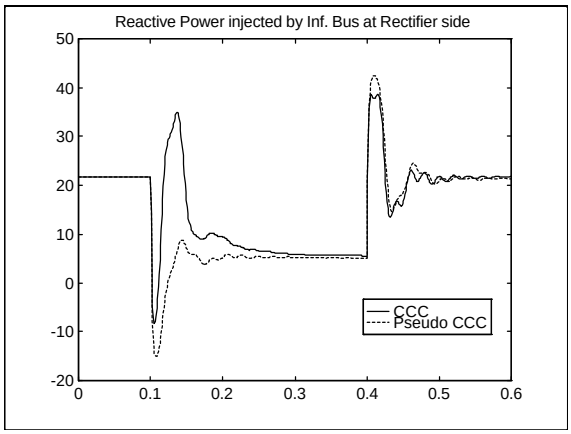

Figure 31 - Reactive Power Injected by Infinite Bus at Rectifier side(Q_{dc1})
Results for Test System 1: CCC versus Pseudo CCC.

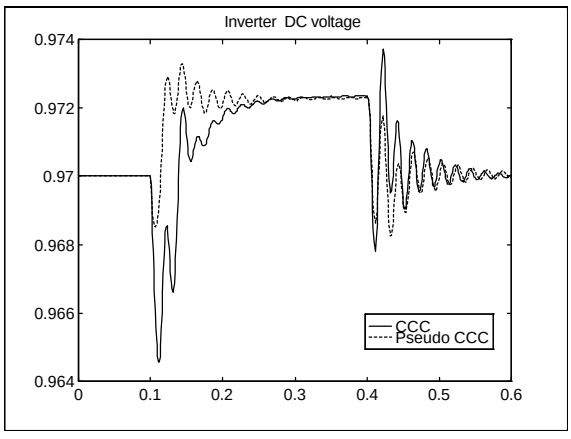

Figure 32 - Inverter DC Voltage (V_{dc2})
Results for Test System 1: CCC versus Pseudo CCC.

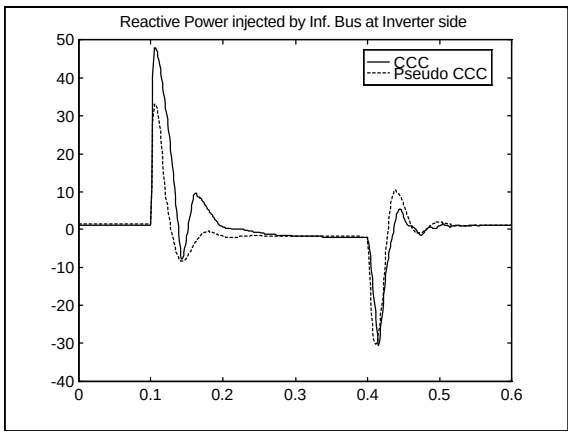

Figure 33 - Reactive Power Injected by Infinite Bus at Inverter side(Q_{dc2})
Results for Test System 1: CCC versus Pseudo CCC.

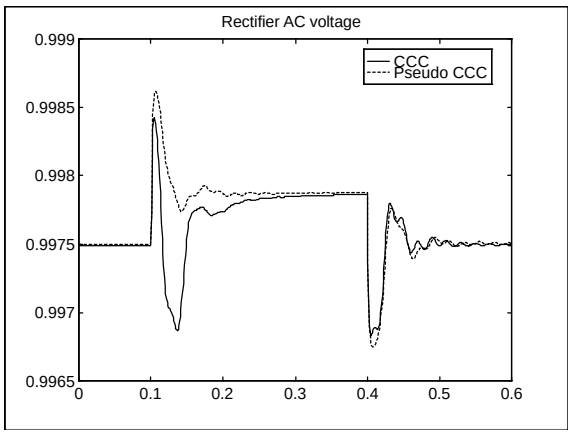

Figure 34 - Rectifier AC Voltage (V_{ac1})
Results for Test System 1: CCC versus Pseudo CCC.

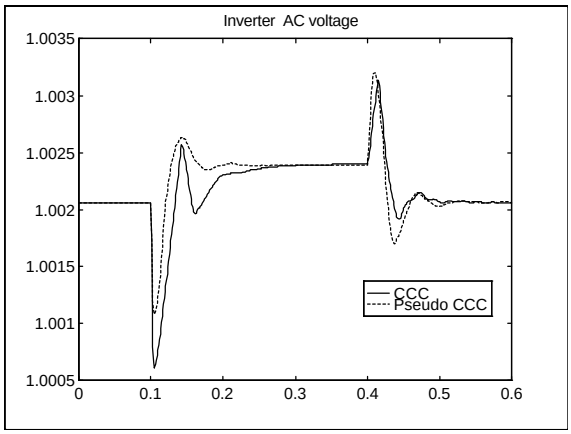

Figure 35 - Inverter AC Voltage (V_{ac2})
Results for Test System 1: CCC versus Pseudo CCC.

8.3 *Results for Test System 2* (*CCC versus Pseudo CCC*)

The use of the conventional converter for Test System 2 is not practical since a high value of shunt capacitance (530 Mvar) would be needed to impose the same boundary power flow conditions as for the CCC. Additionally, the use of a special voltage stabilization control would be needed in order to keep the system stable. For the above mentioned reasons, the results on the conventional converter for Test System 2 are not shown in this paper.

The step disturbance results for the CCC and pseudo CCC models are shown in Figure 36 to Figure 42 for Test System 2. The controller parameters for both models are the same. It is important to note that the parameters were not optimized. The time responses in these figures are self-explanatory and show that, for Test System 2, the pseudo CCC does not present the higher frequency oscillatory mode which is observed in the CCC variable plots.

The pseudo CCC model would not be adequate to model the CCC in transient stability studies for Test System 2 since their dynamics are considerably different.

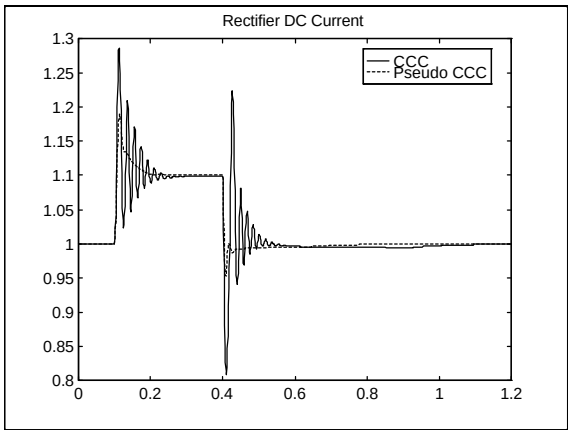

Figure 36 - Rectifier DC Current (I_{dc1}).
Results for Test System 2: CCC versus Pseudo CCC.

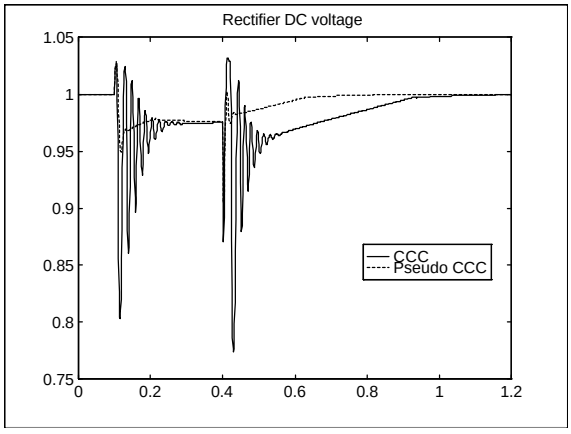

Figure 37 - Rectifier DC Voltage (V_{dc1}).
Results for Test System 2: CCC versus Pseudo CCC.

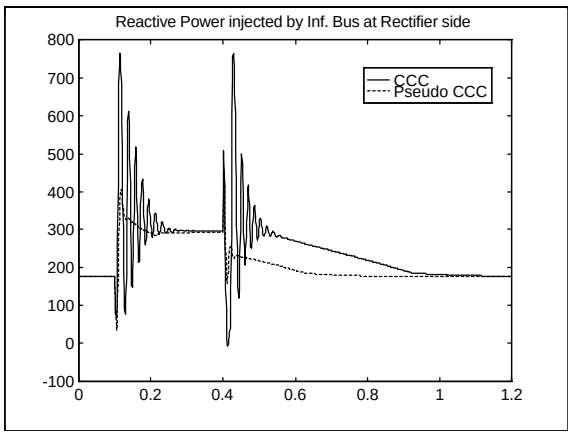

Figure 38 - Reactive Power Injected by Infinite Bus at Rectifier side(Q_{dc1}).
Results for Test System 2: CCC versus Pseudo CCC.

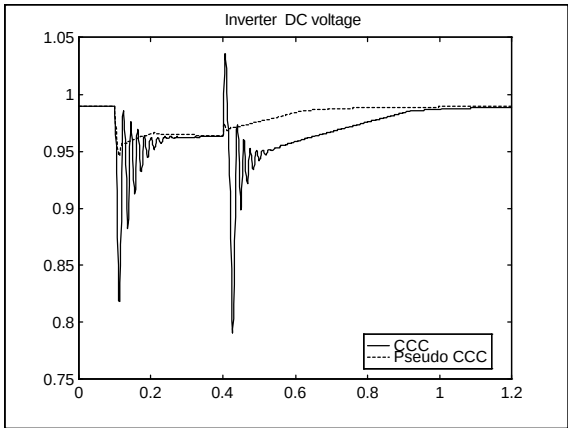

Figure 39 - Inverter DC Voltage (V_{dc2})
Results for Test System 2: CCC versus Pseudo CCC.

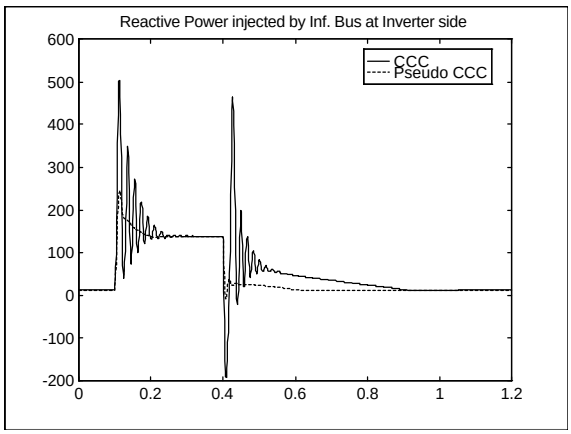

Figure 40 - Reactive Power Injected by Infinite Bus at Inverter side(Q_{dc2})
Results for Test System 2: CCC versus Pseudo CCC.

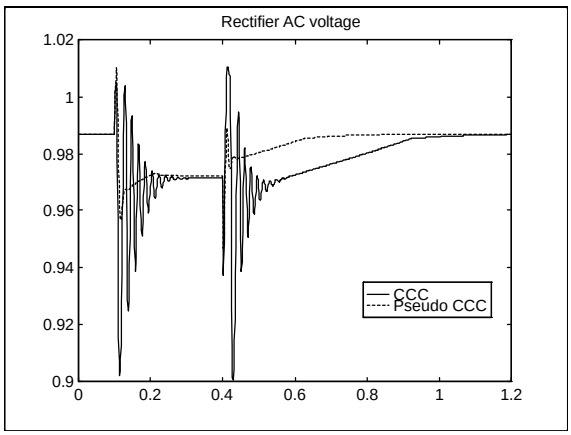

Figure 41 - Rectifier AC Voltage (V_{ac1})
Results for Test System 2: CCC versus Pseudo CCC.

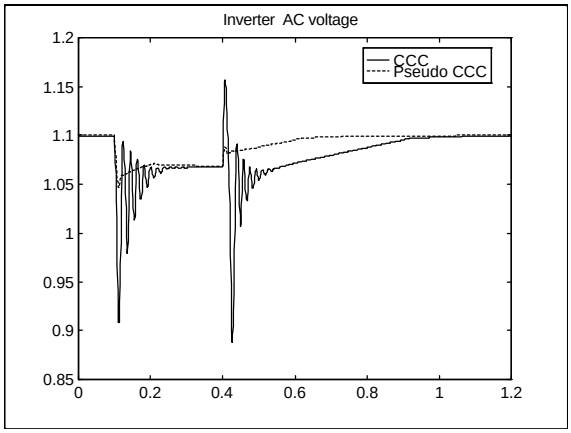

Figure 42 - Inverter AC Voltage (V_{ac2})
Results for Test System 2: CCC versus Pseudo CCC.

9. Conclusion

The CEPEL simulation package allow studies of power flow, transient stability, small signal stability and control design in power systems, considering the detailed models of HVDC links with Capacitor Commutated Converters (CCC).

The paper presents power flow results for two test systems considering five different control modes of operation.

The Root Loci of the system critical eigenvalues were produced by PacDyn for varying gains in the proportional and integral channels of the rectifier current controller. This tool is rather useful when optimizing controller parameters, defining new control strategies or additional stabilizing signals.

Results are presented for transient stability simulations in the ANATEM program, for step disturbances as well as severe AC faults at the inverter. The program showed consistent results with those produced by the PSS/E program, from PTI.

The comparative studies carried out showed the advantages of the CCC over the conventional converter model

particularly in cases involving very weak receiving AC systems (low SCR). This is due to the lower reactive consumption of the CCC as compared to the conventional model during both transient and steady-state conditions.

A comparative study between the CCC and pseudo CCC models was also carried out. In the pseudo CCC model, the capacitor is modeled as a capacitive reactance external to a conventional converter model. The two models presented similar qualitative behaviors, but rather different dynamic performance. These results showed that the detailed CCC equations are necessary to model adequately the converters, mainly when connected to weak AC systems.

The CEPEL software package has already been used in several engineering studies, contracted by ABB Power Systems, involving planned power injections at the Southern part of the Brazilian grid.

Acknowledgments

The authors are grateful to Mr. John Graham (ABB Power Systems) and Mr. Donald Menzies (Furnas Centrais Elétricas), for their valuable strategic and technical support throughout this work.

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[8] **Karlsson, T.; Liss G.** - *HVDC Transmissions with Extremely Long DC Cables Control Strategies*, IEEE/KTH Stockholm Power Tech Conference, Stockolm, Sweden, June 1995.

Appendix 1 - Test System Data

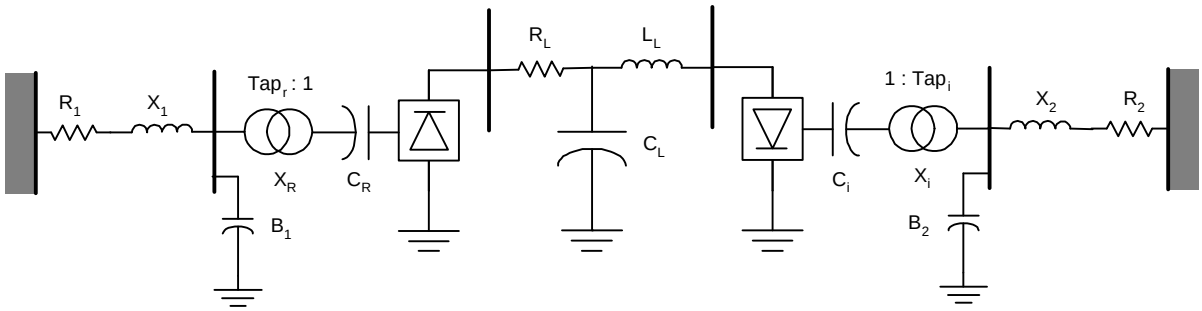

Figure A1.1 - Test System 1 - Long DC Cable Transmission with strong AC systems at both sides

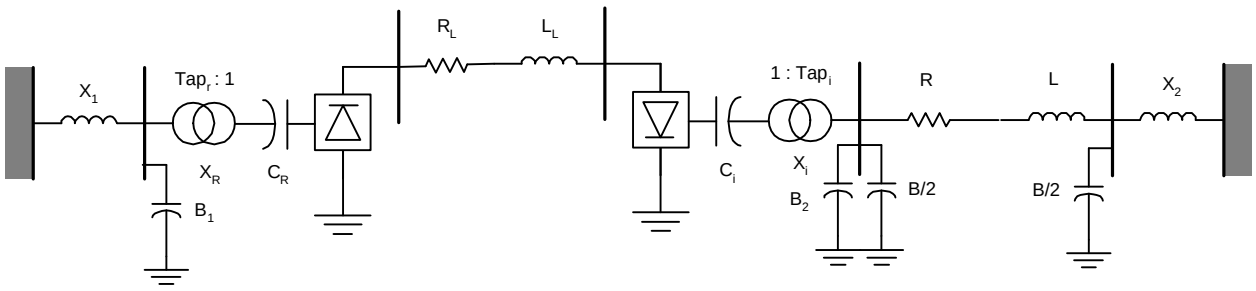

Figure A1.2 - Test System 2 - Back to Back scheme suplying a very weak receiving system (SCR = 1.4)

Data for Test System 1

AC System:

Base: 100 MVA
Infinite AC bus voltages: 1 pu , 0 degrees
$R_1 = R_2 = 0.00033$ pu in a 100 MVA base
$X_1 = X_2 = 0.0033$ pu in a 100 MVA base
$B_1 = B_2 = 84$ Mvar for 1 pu voltage

DC System:

Base: 400 kV , 600 MW
Nominal DC Current: 1500 A
$R_L = 8$ ohms, $L_L = 57$ mH, $C_L = 107\mu F$.
Smoothing Reactor + Earth Resistance for each converter : $R_a = 0.2$ ohms, $L_a = 200$ mH.
Equivalent 6-pulse bridge
Rectifier and Inverter Transformer Data:
Base: $S_b = 625.5$ MVA , V_b (secondary) = 295.2 kV
Reactance: X = 13.1 pu
Rectifier and Inverter Commuted Capacitance: C = 61.55μF, f=50 Hz

Data for Test System 2

AC System:

Rectifier Side:
Base: 100 MVA
Infinite AC bus voltage: 1 pu , 0 degree
$X_1 = X_2 = 0.0147$ pu
$B_1 = 150$ Mvar for 1 pu voltage

Inverter Side
Infinite AC bus voltage: 1 pu , 0 degree
0.0147 pu
$B_2 = 150$ Mvar for 1 pu voltage
R = 0.00374 pu
X = 0.04553 pu
B = 509.1 Mvar for 1 pu voltage

DC System:
Base: 280 kV , 1080 MW
Nominal DC Current: 3860 A
$R_L = 0.8$ ohms, $L_L = 200$ mH (smoothing reactor)
Four 6-pulse bridges (2 bipoles of 12-pulse bridges)
Rectifier and Inverter Transformer Data:
Base: $S_b = 285$ MVA , V_b (secondary) = 52.2 kV
Reactance: X=0.12 pu (for rectifier) , X = 0.144 pu (for inverter)
Rectifier Commuted Capacitance: C = 800μF, f=50 Hz
Inverter Commuted Capacitance: C = 620μF, f=60 Hz

Appendix 2 - Power Flow Results

Power Flow Results for Test System 1

	V (pu)	θ (deg)	P_{ldc} (MW)	Q_{ldc} (Mvar)	Q_{sh} (Mvar)	Tap (pu)	α , γ (deg)	U_d (pu)	μ (deg)	I_d (pu)
Case1- Rect.	0.997	-1.1	600.5	93.4	83.6	0.979	**1.00**	**1.000**	14.47	**1.00**
Case1- Inv.	1.002	1.1	-581.5	74.5	84.3	1.019	**17.00**	0.970	15.50	1.00
Case2- Rect.	0.995	-1.1	600.5	174.1	83.1	**0.950**	10.22	**1.000**	11.33	**1.00**
Case2- Inv.	1.002	1.1	-581.5	74.5	84.3	1.019	**17.00**	0.970	15.50	1.00
Case3- Rect.	0.998	-1.0	583.7	91.2	83.6	1.007	**1.00**	0.972	14.57	**1.00**
Case3- Inv.	1.002	1.0	-564.8	68.9	84.4	**1.050**	**17.00**	0.942	15.82	1.00
Case4- Rect.	0.995	-1.1	583.7	163.7	83.2	**0.980**	9.54	0.972	11.65	**1.00**
Case4- Inv.	1.002	1.1	-564.8	68.9	84.4	**1.050**	**17.00**	0.942	15.82	1.00
Case5- Rect.	1.000	-1.0	539.8	22.0	84.0	**1.080**	**-8.90**	0.917	19.62	**0.98**
Case5- Inv.	0.998	1.0	-521.6	193.0	83.7	**1.050**	31.02	0.888	10.58	0.98

The highlighted cells in these tables indicate user specified values and the others indicate calculated values

Power Flow Results for Test System 2

	V (pu)	θ (deg)	P_{ldc} (MW)	Q_{ldc} (Mvar)	Q_{sh} (Mvar)	Tap (pu)	α , γ (deg)	U_d (pu)	μ (deg)	I_d (pu)
Case1- Rect.	0.987	-9.3	1080.0	146.0	146.1	0.983	**1.00**	**1.000**	12.55	**1.00**
Case1- Inv.	1.100	33.8	-1068.1	126.9	181.5	1.109	**20.00**	0.989	14.84	1.00
Case2- Rect.	0.975	-9.4	1080.0	221.9	142.5	**0.960**	5.79	**1.000**	11.06	**1.00**
Case2- Inv.	1.100	33.8	-1068.1	126.9	181.4	1.109	**20.00**	0.989	14.84	1.00
Case3- Rect.	0.987	-9.3	1080.0	146.8	146.1	1.001	**1.00**	0.982	12.65	**1.00**
Case3- Inv.	1.118	33.1	-1067.6	115.7	187.4	**1.150**	**20.00**	0.970	15.24	1.00
Case4- Rect.	0.966	-9.5	1080.0	272.1	140.1	**0.960**	8.71	0.982	10.41	**1.00**
Case4- Inv.	1.118	33.1	-1067.6	115.7	187.4	**1.150**	**20.00**	0.970	15.24	1.00
Case5- Rect.	1.013	-7.5	896.6	6.5	153.9	**1.200**	**-8.90**	0.847	16.84	**0.98**
Case5- Inv.	1.003	30.8	-885.1	279.1	150.9	**1.150**	32.47	0.836	11.50	0.98

The highlighted cells in these tables indicate user specified values and the others indicate calculated values

Appendix 3 - Comparison Between PSS/E and ANATEM Results

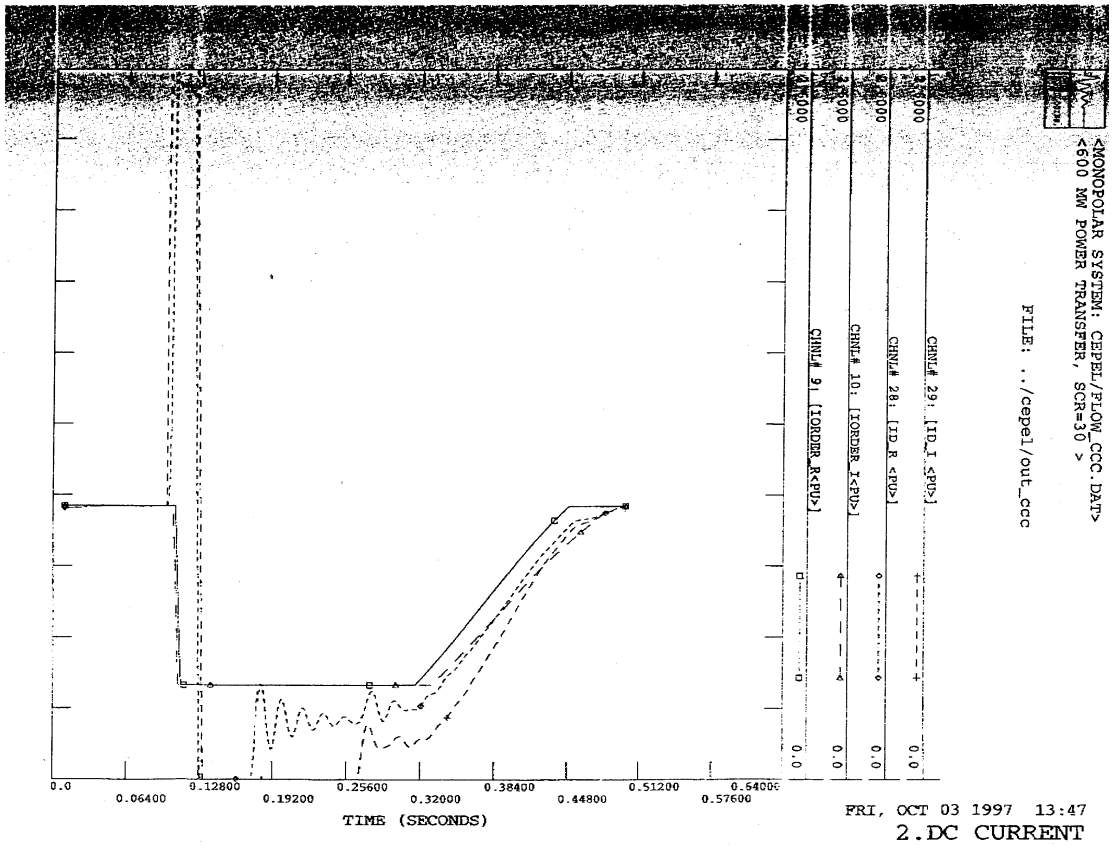

Figure A3-1 - FAX transmission by ABB with the plots of rectifier DC current, inverter DC current, rectifier current order limited by VDCOL and inverter current order limited by VDCOL from simulation performed in the PSS/E program for a three [illegible]

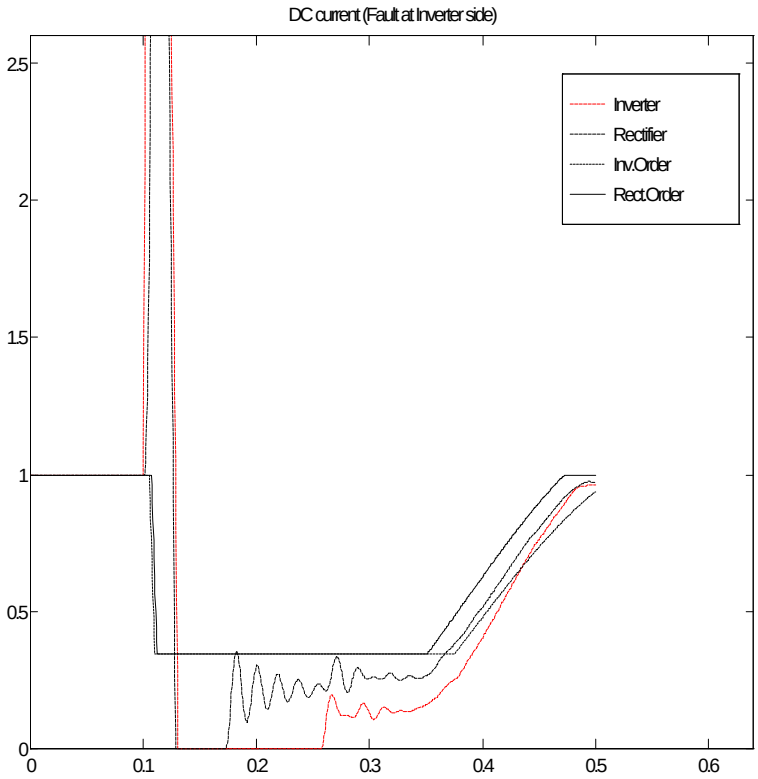

Figure A3-2 - Plots of rectifier DC current, inverter DC current, rectifier current order limited by VDCOL and inverter current order limited by VDCOL from simulation performed in ANATEM program for a three phase fault at inverter side. Note: The rectifier DC current plot of this figure is shown on a different scale in Figure 11.